An All-Digital CMOS Pulse-Shrinking Mechanism for Time Measurement

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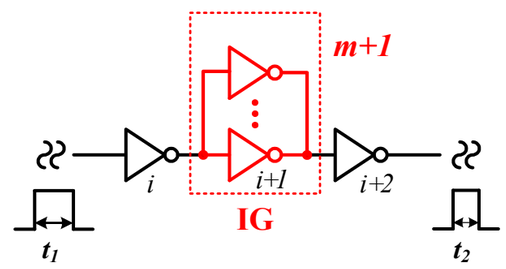
Abstract

This paper presents a newly developed all-digital CMOS pulse-shrinking mechanism for time measurement, aimed at enhancing time resolution and improving circuit performance under process and temperature variations. In the previous all-digital mechanism, the pulse-shrinking amount (time resolution) was determined by adjusting the number of NOT gates in the inhomogeneous stage to achieve sub-gate resolution. The new mechanism introduces buffer gates to replace the original NOT gates, with the NOT gates simply added in the inhomogeneous stage to form these buffer gates. An analysis of the resolution is provided, demonstrating that the buffer-based technique effectively improves resolution compared to the inverter-based approach. The all-digital CMOS mechanism was implemented using a 0.35-μm CMOS TSMC process for performance evaluation. Simulation results show that the proposed mechanism achieves significant resolution improvement with greater stability against process and temperature variations.

All-Digital Mechanism

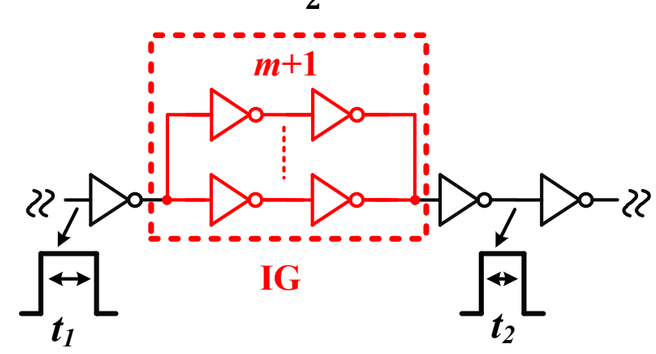


All-digital inverter-based pulse-varying mechanism

$$r = (m+1-\frac{1}{m+1}) \times \eta,\ \eta = C_i(\frac{1}{k_{P_i}} - \frac{1}{k_{N_i}}) \times \varphi$$

$$\eta = 2C_{OX}WL \times (\frac{1}{\mu_P C_{OX}\frac{W}{L}} - \frac{1}{\mu_P C_{OX}\frac{W}{L}}) \times \phi = L^2 \times 2(\frac{1}{\mu_P} - \frac{1}{\mu_N}) \times \phi$$

Best Resolution $= \frac{3}{2} \times \eta$ **(*m*=1)**

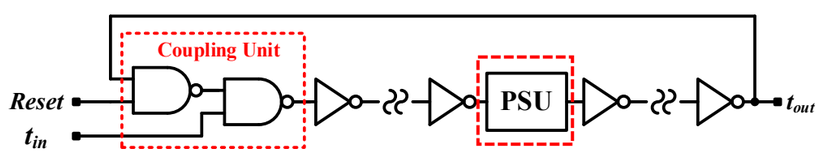


All-digital buffer-based pulse-shrinking mechanism

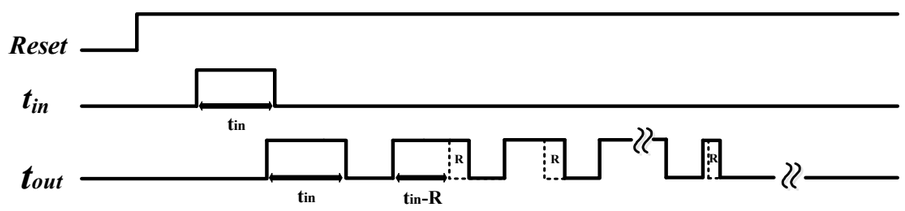
$$r = \left(m+1+\frac{1}{m+1}-2\right) C_i \left(\frac{1}{k_{P_i}} - \frac{1}{k_{N_i}}\right) \times \varphi$$
$$= \left(\frac{m^2}{m+1}\right) C_i \left(\frac{1}{k_{P_i}} - \frac{1}{k_{N_i}}\right) \times \varphi$$

Best Resolution $= \frac{1}{2} \times \eta$ **(*m*=1)**

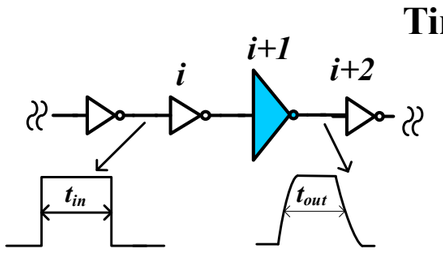
Full-Custom Mechanism



TDC with a PSU



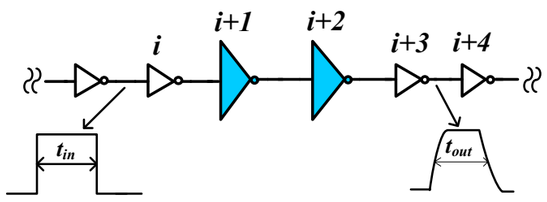
Timing Diagram



$$r = (\beta - \frac{1}{\beta}) C_i (\frac{1}{k_{P_i}} - \frac{1}{k_{N_i}}) \times \varphi$$

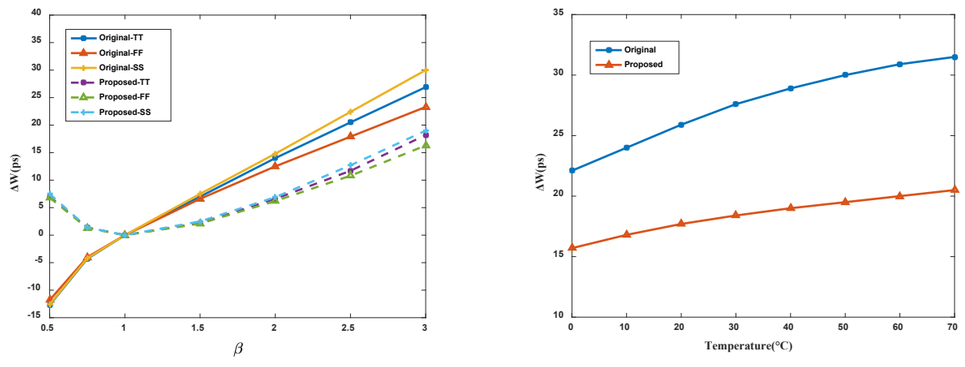
$$\varphi = \left[\frac{2V_{th}}{(V_{DD}-V_{th})^2} + \frac{1}{V_{DD}-V_{th}} \ln\left(\frac{1.5V_{DD}-2V_{th}}{0.5V_{DD}}\right)\right]$$

Full-Custom inverter-based mechanism



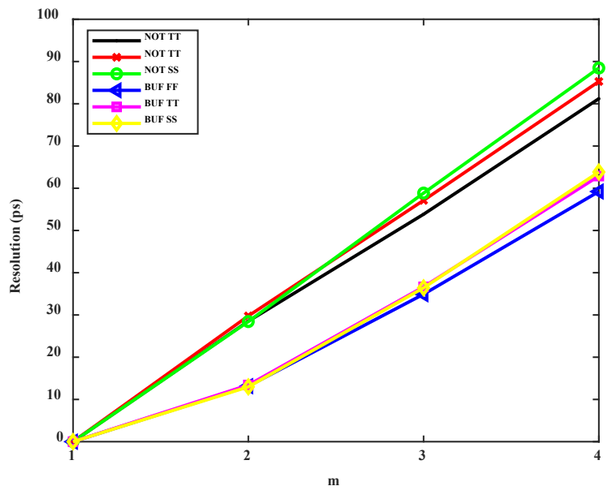
$$r = \left(\beta + \frac{1}{\beta} - 2\right) C_i \left(\frac{1}{k_{P_i}} - \frac{1}{k_{N_i}}\right) \times \varphi$$

Full-Custom buffer-based mechanism

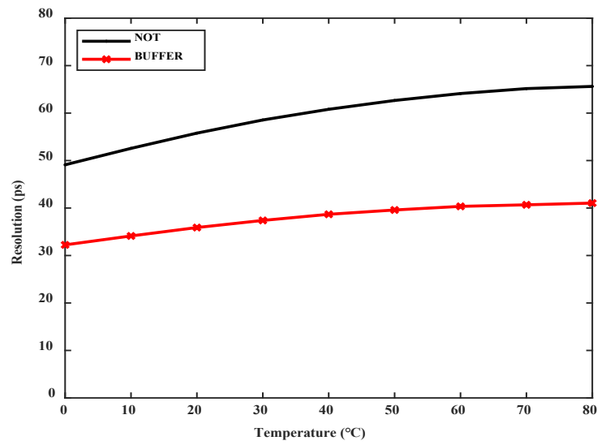


Results of the two full-custom mechanisms

Experimental Results



Simulated resolutions for different *m* value and process



Simulated results for temperature variation

Performance Comparison

Mechanism	Resolution (ps)	Fluctuation (Process Var.) (%)	Fluctuation (Temp. Var.) (%)
Inverter-based	57	±4	±14
Buffer-based	36	±2	±12